ABSTRACT OF THE DISCLOSURE

In a semiconductor memory device equipped with a memory cell array in which dynamic memory cells are arrayed, for example, in a matrix, a technique speeds up of a read operation. In the read cycle, an external access controller outputs an external access execution timing signal which changes to active after the change of the output enable signal to active, and changes to inactive after a start of the latch of the read signal caused by changes of the latch signal to active and inactive. In the read cycle, the refresh controller outputs the refresh execution timing signal which changes to active according to the change of the latch signal to active while the refresh requirement signal is active, and stays active for a predetermined time period.